

ABSTRACT OF THE DISCLOSURE

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A mask identification (ID) bit circuit (100) is disclosed that provides one of two potentials (VGND or VPWR) to a sense node (108). A mask ID bit circuit (100) may include a number of links (102-0 to 102-4) arranged in series. A link (102-0 to 102-4) may include
5 inputs (104-0 and 104-1) and outputs (106-0 and 106-1). In one configuration, inputs (104-0 and 104-1) may be directly coupled to outputs (106-0 and 106-1). In another configuration, inputs (104-0 and 104-1) may be cross coupled to outputs (106-0 and 106-1). Cross coupling inputs (104-0 and 104-1) and outputs (106-0 and 106-1) of a link (102-0 to 102-4) can switch a potential (VGND or VPWR) supplied to a sense node (108). The configuration of more
10 than one link (102-0 to 102-4) of a mask ID bit circuit (100) can be changed, allowing a sense node to be switched between two potential (VGND and VPWR) multiple times. According to an embodiment, n mask ID bit circuits (100) may provide as many as 2^n different mask ID codes.